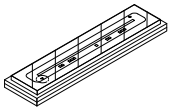
NOP04811

400/300/200/100 DPI High-Speed Photodiode Array

ON Semiconductor®

http://onsemi.com



OLCC12
CL SUFFIX
CASE 755AA

Description

The NOP04811 photodiode array (PDA) provides selectable 400, 300, 200 and 100 dot per inch (dpi) resolution. The sensor contains an on−chip output amplifier, internal power−down capability and parallel transfer features that are uniquely combined with advanced active−pixel−sensor technology. Applications for the photodiode sensor array include currency verification, bar code scanning and industrial process automation equipment.

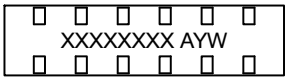
Features

- 400, 300, 200 and 100 dpi Selectable Resolutions
- 232, 174, 116 or 58 Image Sensor Elements (pixels)
- 63.45 μm (400 dpi) Pixel Center−to−Center Spacing
- On−chip Amplifier
- Single 3.3 V Power Supply
- 3.3 V Input Clocks and Control Signals
- 8.0 MHz Maximum Pixel Rate
- Parallel Integration and Transfer Operations
- Automatic Power−down of Internal Circuitry
- High Sensitivity
- Low Power
- Low Noise
- This is a Pb−Free Device

Applications

- Currency Verification
- Document Scanning
- Barcode Scanning
- Process Automation Equipment

MARKING DIAGRAM



(Bottom View of Package)

XXXXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

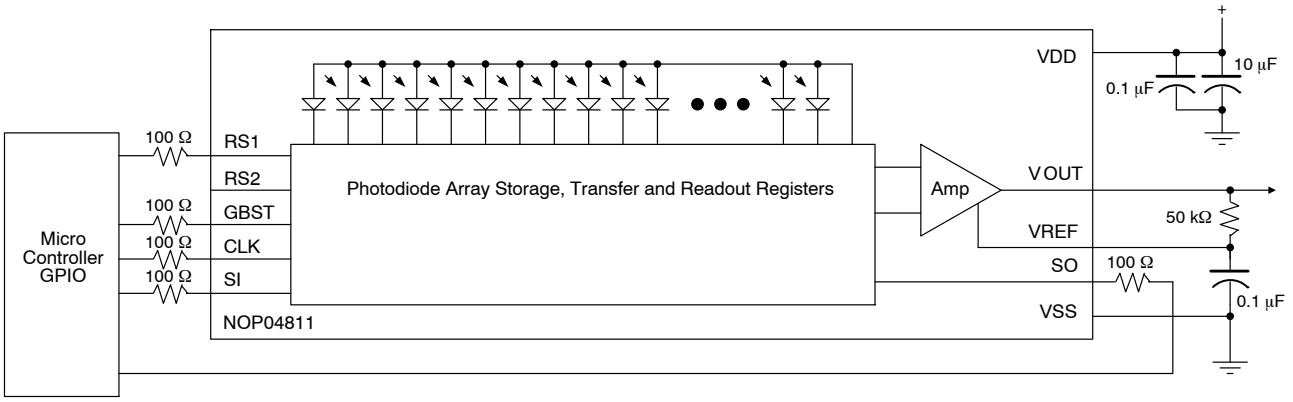


Figure 1. Typical Application Circuit

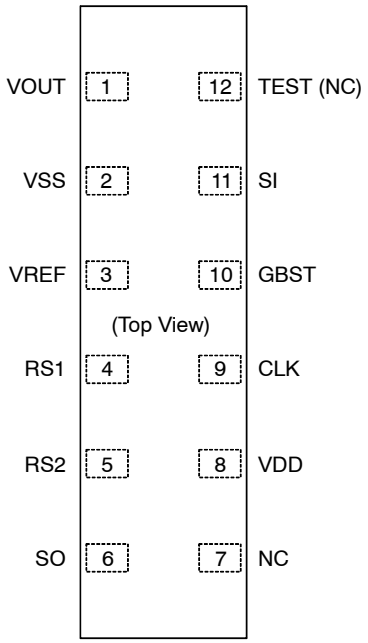


Figure 2. Pinout Configuration

Table 1. PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	VOUT	Analog video output signal
2	VSS	Ground
3	VREF	Input reference voltage for the differential amplifier driving VOUT, sets the output reset (dark) voltage level
4	RS1	Selects the 400, 300, 200 or 100 dpi resolution mode
5	RS2 (NC)	Has no functionality, this pad should be left unconnected
6	SO	End−of−scan output pulse used to drive the start pulse (SI) input of the next sensor chip in a module
7	NC	No connect, this pad should be left unconnected
8	VDD	+3.3 V power supply
9	CLK	Clock input for the shift register
10	GBST	Global start pulse initializes the start inputs of all sensor chips in a module and starts the scanning process of the first sensor chip
11	SI	Start pulse, input to start a line scan
12	TEST (NC)	Test pad used during wafer sort, this pad should be left unconnected

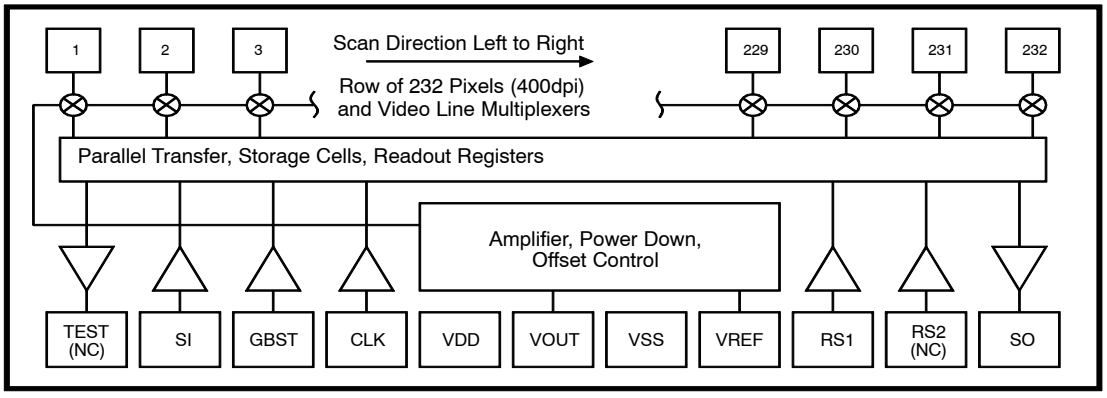


Figure 3. Simplified Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power supply voltage	V_{DD}	4	V
Input voltage range for CLK, SI, GBST, RS1, VREF	V_{in}	V_{SS}−0.5 to V_{DD}+0.5	V
Storage Temperature	T_{STG}	−25 to 75	°C
Storage Humidity, Non−Condensing	H_{STG}	10 to 90	%
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2500	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	250	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78

Table 3. RECOMMENDED OPERATING RANGES (Unless otherwise specified, these specifications apply T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	3.1	3.3	3.5	V
Power supply current, initialization − first 100 clock cycles	I_{DD_INIT}		5.8		mA
Power supply current, integration and transfer mode	I_{DD_OPER}		40		mA
Power supply current, idle mode, still integrating	I_{DD_IDLE}		3.2		mA
Low level input voltage for CLK, SI, GBST, RS1	V_{IL}	V_{SS} − 0.5		0.6	V
High level input voltage for CLK, SI, GBST, RS1	V_{IH}	2.8		V_{DD} + 0.1	V
Reference voltage	V_{REF}	1.1	1.2	1.3	V
Clock frequency	f	0.5	8.0	8.0	MHz
Pixel rate (Note 2)	P_R	0.5	8.0	8.0	MHz
Integration time (line scan rate) (Note 3)	T_{int}			99.5	μs
Resistive load on VOUT	R_L	50	50		kΩ
Capacitive load on VOUT	C_L			150	pF
Operating Temperature	T_{op}	−10		50	°C
Operating Humidity, Non−Condensing	H_{op}	10		85	%

2. One pixel is clocked out for every clock cycle.
3. Tint is the integration time of a single sensor and is the time between two start pulses. The minimum integration time is the time it takes to clock out 100 inactive pixels and 232 active pixels for the 400 dpi mode, 100 inactive pixels and 174 active pixels for the 300 dpi mode, 100 inactive pixels and 116 active pixels for the 200 dpi mode or 100 inactive pixels and 58 active pixels for the 100 dpi mode, at a given frequency.

Table 4. PHYSICAL SPECIFICATIONS

Parameter	Symbol	Typ	Unit
Number of pixels, 400 dpi	P_{n_400}	232	
Number of pixels, 300 dpi	P_{n_300}	174	
Number of pixels, 200 dpi	P_{n_200}	116	
Number of pixels, 100 dpi	P_{n_100}	58	
Pixel−to−pixel spacing, 400 dpi	D_{pp_400}	63.45	μm
Pixel−to−pixel spacing, 300 dpi	D_{pp_300}	84.60	μm
Pixel−to−pixel spacing, 200 dpi	D_{pp_200}	126.90	μm
Pixel−to−pixel spacing, 100 dpi	D_{pp_100}	253.80	μm

Table 5. SWITCHING CHARACTERISTICS (Unless otherwise specified, these specifications apply T_A = 25°C) (Note 4)

Parameter	Symbol	Min	Typ	Max	Unit
CLK clock period (Note 5)	t_o		125	2000	ns
CLK pulse width (Note 5)	t_w		62.5		ns
CLK duty cycle (Note 6)	DC_{CLK}	45	50	55	%
GBST setup time (Notes 5, 7)	t_{su}	20			ns
GBST hold time (Notes 5, 7)	t_h	25			ns
CLK rise time (Notes 5, 8)	t_{r_CLK}			62.5	ns
CLK fall time (Notes 5, 8)	t_{f_CLK}			62.5	ns
GBST rise time (Notes 5, 8)	t_{r_GBST}			62.5	ns
GBST fall time (Notes 5, 8)	t_{f_GBST}			62.5	ns
Pixel output timing, CLK = 8 MHz	TS	75			ns
Pixel output rise time (Note 9)	P_{rt}		TBD		ns

4. Refer to Figure 4 through Figure 6 for more information on AC characteristics
5. Assuming a 50% duty cycle.
6. Defined as the ratio of the positive duration of the clock to its period.
7. The shift register loads on the falling edge of CLK, therefore setup and hold times (tsu, th) are needed to prevent loading of multiple start pulses. This would occur if GBST remains high during two fallings edges of the CLK signal. See Figure 4.
8. Clock rise time should match clock fall time.
9. Pixel output rise time measured at 8 MHz with 150 pF and 50 kΩ load to ground with the output at saturation.

Table 6. ELECTRO−OPTICAL CHARACTERISTICS TEST CONDITIONS

Parameter	Symbol	Value	Unit
Power supply voltage	V_{DD}	3.3	V
Reference voltage	V_{REF}	1.2	V
Clock frequency	f	8.0	MHz
Clock pulse duty cycle	DC_{CP}	50	%
Integration time, 400 dpi	T_{int_400}	41.5	μS
Integration time, 300 dpi	T_{int_300}	34.25	μS
Integration time, 200 dpi	T_{int_200}	27.0	μS
Integration time, 100 dpi	T_{int_100}	19.75	μS
Resistive load on VOUT (Note 10)	R_L	50	kΩ
Capacitive load on VOUT (Note 11)	C_L	150	pF
Average output voltage swing (Note 12)	V_{avg}	1.0	V
LED peak wavelength (Note 13)	λ_p	550	nm
Operating Temperature	T_{op}	25	°C

10. Resistive load connected between VOUT and VREF. VREF is typically has a lower noise level than VSS.
11. Capacitive load connected between VOUT and VSS.
12. The average output voltage Vavg is defined as the voltage difference between the average pixel level in the light and the average pixel level in the dark. It should be adjusted to approximately 1.0 V, unless stated otherwise.
13. A linear array of uniform green LEDs acts as the light source for measurements requiring illumination, unless otherwise stated.

Table 7. ELECTRO−OPTICAL CHARACTERISTICS
(Unless otherwise specified, these specifications were achieved with the test conditions defined in Table 6)

Parameter	Symbol	Min	Typ	Max	Unit
Dark output voltage (Note 14)	V_d	V_{REF} − 0.150	V_{REF}	V_{REF} + 0.150	V
Dark output non−uniformity (Note 15)	U_d	0		100	mV
Photo−response non−uniformity (Note 16)	U_p	−15		15	%
Adjacent pixel photo−response non−uniformity (Note 17)	U_{padj}	0		15	%
Saturation voltage (Note 18)	V_{Sat}		1.2		V
Sensitivity, 400 dpi (Note 19)	S_{V_400}		2135		V/μJ/cm^2
Sensitivity, 300 dpi (Note 19)	S_{V_300}		TBD		V/μJ/cm^2
Sensitivity, 200 dpi (Note 19)	S_{V_200}		TBD		V/μJ/cm^2
Sensitivity, 100 dpi (Note 19)	S_{V_100}		TBD		V/μJ/cm^2
Photo−response linearity (Note 20)	PRL	99		107	%
Individual rms pixel noise, 400 dpi (Note 21)	$P_{\_noise}$	0	3	15	mV
Image lag (chip average) (Note 22)	IL			1	%

14. Vd is the average dark output level and represents the offset level of the video output in the dark. The dark level is set by VREF and is recommended to be 1.2 V for optimal module operation.
15. Ud = Vdmax − Vdmin, where
    Vdmax is the maximum pixel output voltage in the dark
    Vdmin is the minimum pixel output voltage in the dark
    In the 400 dpi mode, dark output non−uniformity is tested at 4 ms.
16. Up = [(Vpmax − Vpavg)/Vpavg] x 100%, or [Vpavg − Vpmin)/Vpavg] x 100%, whichever is greater, where
    Vpmax is the maximum pixel voltage of any pixel at full bright
    Vpmin is the minimum pixel voltage of any pixel at full bright
    Vpavg is average output voltage of all pixels at full bright.
17. Upadj = MAX [| (Vp(n) − Vp(n+1) | / Vpavg] x 100%, where
    Upadj is the nonuniformity in percent between adjacent pixels for a bright background
    Vp(n) is the pixel output voltage of pixel n at full bright.
18. VSat is defined as the maximum video output voltage swing measured from the dark level to the saturation level. It is measured by using the module LED light source with the module imaging a uniform white target. The LED light level is increased until the output voltage no longer increases with an increase in the LED brightness.
19. Sv is defined as the slope of the Vpavg vs. Exposure curve. Sensitivity uniformity is nominally better than ±10% die−to−die.
20. PRL = ((Vratio − Tratio) / Tratio) x 100%, where
    Vratio = (Vavg3 − Vavg1) / (Vavg2 − Vavg1)
    Tratio = (Tint3 − Tint1) / (Tint2 − Tint1)
    Tint1 is the integration time needed to get a Vavg1 of about 0.1 V
    Tint2 is the integration time needed to get a Vavg2 of about 0.5 V
    Tint3 is the integration time needed to get a Vavg3 of about 0.9 V
    A specification limit of 5% for this test method is a tighter spec than ±5% deviation from a best fit line. Linearity is specified within the range of the saturation voltage.
21. Individual rms pixel noise is defined as the standard deviation of each pixel in the dark. This can also be considered output referred noise as it is measured at the sensor output.
22. Image lag is defined as taking two subsequent CIS reads where the first readout occurs when the sensor is illuminated such that the imager output voltage is in saturation and the second readout occurs with zero irradiance falling on the sensor.

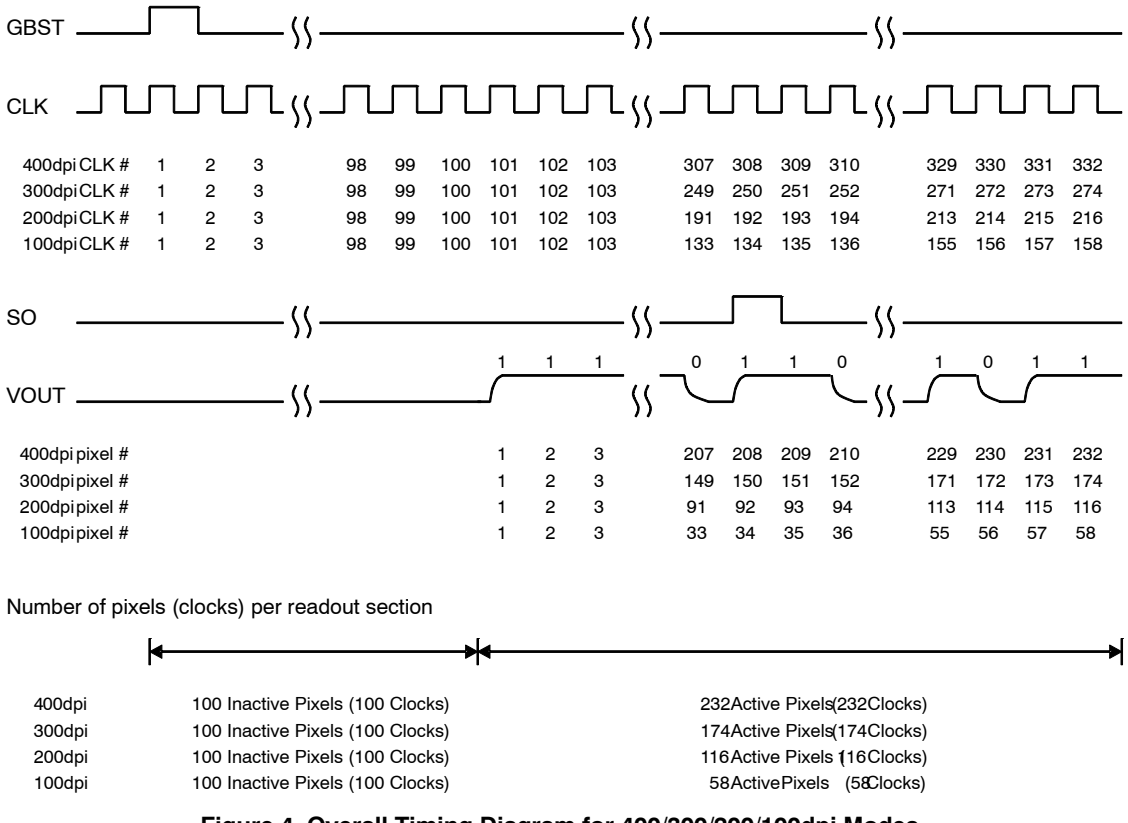


Figure 4. Overall Timing Diagram for 400/300/200/100dpi Modes

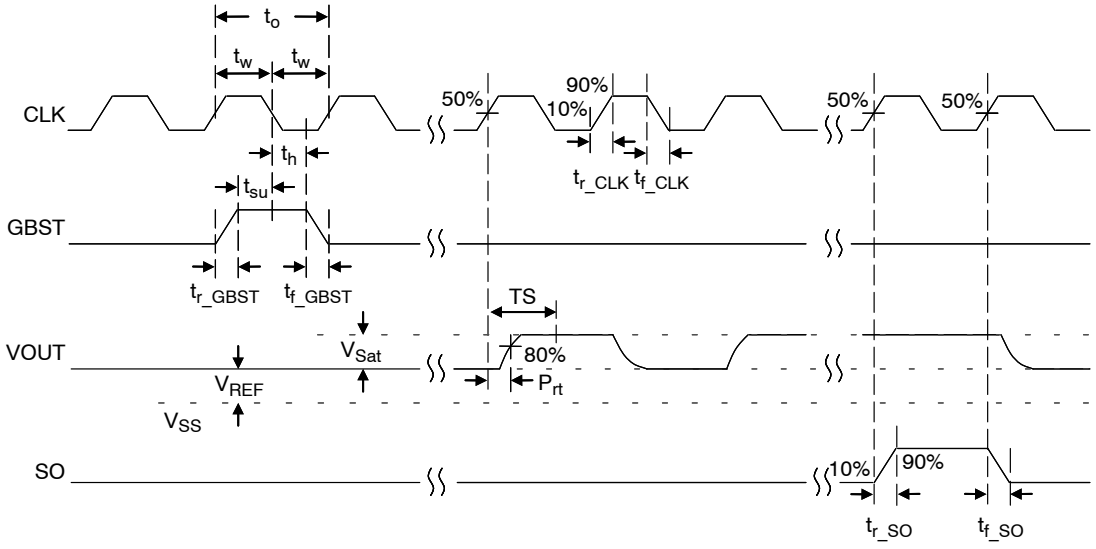


Figure 5. Rise and Fall Times for 400/300/200/100dpi Modes

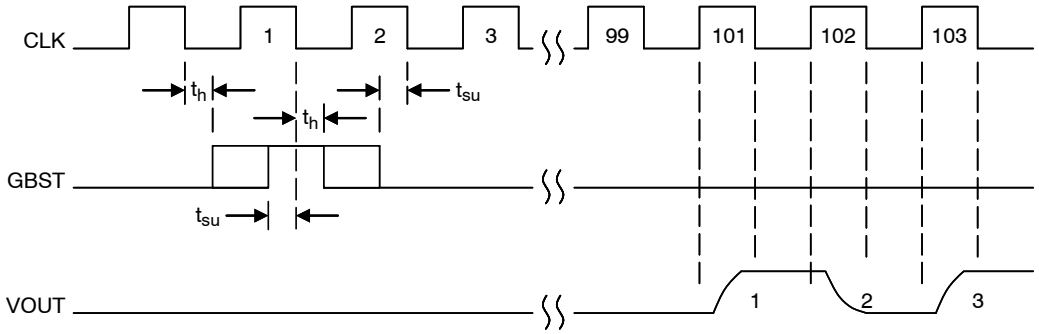
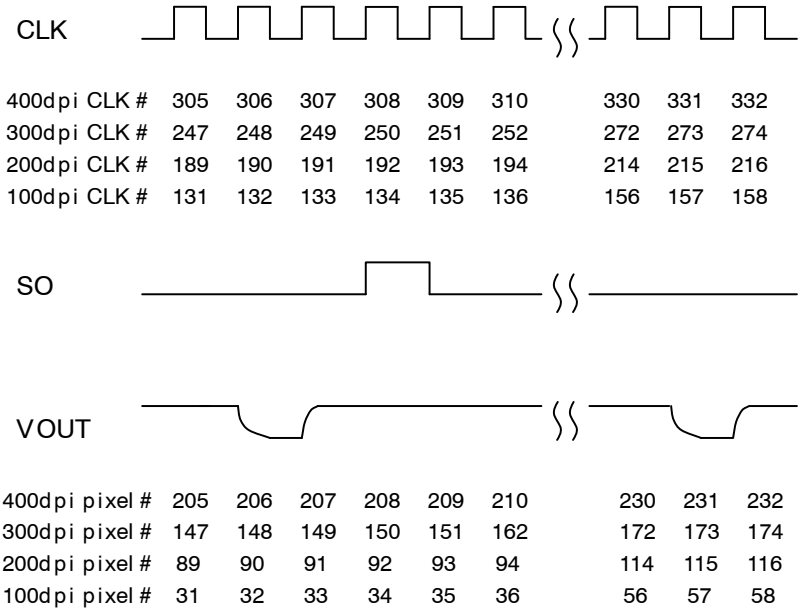


Figure 6. Timing of GBST−to−First Pixel for 400/300/200/100 dpi Modes



400dpi CLK #	305	306	307	308	309	310	330	331	332
300dpi CLK #	247	248	249	250	251	252	272	273	274
200dpi CLK #	189	190	191	192	193	194	214	215	216
100dpi CLK #	131	132	133	134	135	136	156	157	158

400dpi pixel #	205	206	207	208	209	210	230	231	232
300dpi pixel #	147	148	149	150	151	162	172	173	174
200dpi pixel #	89	90	91	92	93	94	114	115	116
100dpi pixel #	31	32	33	34	35	36	56	57	58

Figure 7. Timing of SI/SO Clock for 400/300/200/100 dpi Modes

Description of Operation

Functional Description

The NOP04811 photodiode array has selectable 400, 300, 200 and 100 dpi resolution. The sensor contains an on−chip output amplifier, automatic power−down circuitry and parallel transfer features that are uniquely combined with advanced active−pixel−sensor technology. The image photodiode array is designed to be part of an image acquisition system including the necessary optical lens as illustrated Figure 1.

Figure 3 is a block diagram of the sensor. Each sensor consists of 232 active pixels, their associated multiplexing switches, buffers and an output amplifier circuit with power down. The pixel−to−pixel spacing is 63.45 μm.

There are a number of features incorporated into the NOP04811 which improve the sensor's performance.

Active Pixel Technology

Active pixel technology supplements the primary photodiode sensor element with additional transistors which condition, amplify and buffer the original signal. Figure 8 illustrates a pair of active pixel cells connected to the internal scan line.

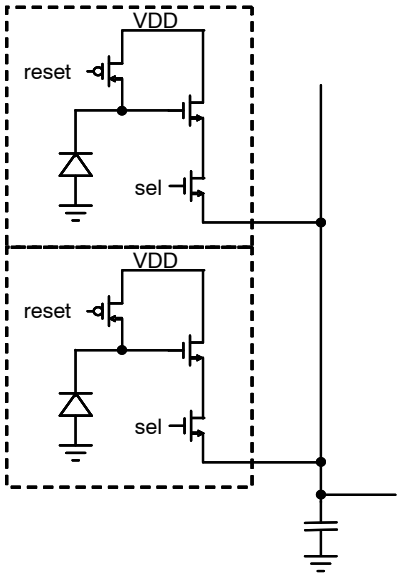


Figure 8. Active Pixel Cell Architecture

Pixel−to−Pixel Offset Cancellation Circuit

The sensor employs a pixel−to−pixel offset cancellation circuit, which reduces the fixed pattern noise (FPN) and amplifier offsets. This innovative circuit design greatly improves the optical linearity and low noise sensitivity.

Parallel Integrate, Hold and Transfer

The sensor has a parallel integrate, transfer and hold feature which allows the sensor to scan data out while photon integration is taking place. These features are approached through the use of an integrate−and−hold cell located at each pixel site. Each pixel's charge is read from its storage site as the shift register sequentially selects each pixel and transfers each pixel's charge onto a common video line.

Scan Initiation Inputs GBST and SI

The sensor has two scan initiation inputs, the global start pulse (GBST) and the start pulse (SI) which are compatible with standard 3.3 V CMOS signal levels. The scan cycle starts when GBST is captured on the falling edge of the clock input (CLK). During the first 100 clock cycles following a GBST pulse, all the pixels cycle through their pre−scan initialization process that reduces FPN and reset noise.

SI selects when an individual sensor is selected. By permanently asserting the SI pin, the scanning sequence is properly initialized. The sensor clocks out 100 inactive pixels before accessing its first active pixel. During these 100 clock cycles, the sensor cycles through the pre−scan initialization process. After initialization, the sensor starts its read cycle with its first−active pixel appearing on the 100th clock cycle.

Power Saving Mode

The sensor incorporates an internal power−saving feature. When the SI pin of a particular sensor is selected for read out, the sensor powers up the output amplifier and then powers it down when the read scan is completed.

Common Reference Voltage

The sensor has an input bias control (VREF), which serves as an offset voltage reference for the output amplifier. In multiple chip operation, the VREF inputs are tied together such that each sensor references the same bias level.

Selectable Resolutions of 400, 300, 200 and 100 dpi

The select resolution input (RS1) is used to select between 400, 300, 200 and 100 dpi modes.

- For 400 dpi, the RS1 input is held high (Vdd)
- For 300 dpi, the RS1 input is held low (Vss)
- For 200 dpi, the RS1 input is held low for clocks 20, 21 and 22 and then high for clocks 44, 45 and 46
- For 100 dpi, the RS1 input is held high for clocks 20, 21 and 22 and then low for clocks 44, 45 and 46

In 400 dpi mode, all 232 pixels are clocked out. In the 300 dpi mode, pixels 1 and 1/2 of pixel 2 are combined, 1/2 of pixel 2 and 3 are combined. Pixel 4 and 1/2 of pixel 5 are combined and 1/2 of pixel 5 and pixel 6 are combined and so on up to 1/2 of pixels 231 and 232 being combined. This will give a net pixel count of 232 pixels. Similarly, in 200 dpi mode, pixels 1 and 2 are combined and pixels 3 and 4 are combined and so on up to pixels 231 and 232 being combined. In 100 dpi mode, pixels 1, 2, 3 and 4 are combined, pixels 5, 6, 7 and 8 are combined and so on up to pixels 229, 230, 231 and 232 being combined.

In the 300 dpi mode, one quarter of the pixel amplifiers and one quarter of the scanning register are disabled when compared to the 400 dpi mode. As a result, sensitivity in the 300 dpi mode will be 1.5 times that of the 400 dpi mode. The 300 dpi readout time will be approximately three quarters of the 400 dpi readout time. Similarly, in 200 dpi mode one half of the pixel amplifiers and one half of the scanning registers are then disabled. As a result, sensitivity in the 200 dpi mode will be twice that of the 400 dpi mode. The 200 dpi readout time will be approximately a half of the 400 dpi readout time. In the 100 dpi mode three quarters of the pixel amplifiers and three quarters of the scanning registers are disabled. Sensitivity in 100 dpi mode is four times the sensitivity in 400 dpi mode. The 100 dpi readout time will be approximately one quarter of the 400 dpi readout time. Unlike a CCD array, the 400 dpi, 300 dpi, 200 dpi and 100 dpi modes all operate at the same clock frequency.

Timing

Figure 4 shows the initialization of the sensor for the 400 dpi, 300 dpi, 200 dpi and 100 dpi modes. The sensor will operate with 100 inactive pixels being clocked out before its first active pixel is clocked out.

Figure 4 and Figure 5 detail the timing of the CLK, GBST, OUT, and SI/SO signals in further detail, they have the same timing requirements for the 400, 300, 200 and 100 dpi modes. The rise and fall times are listed in Table 5. In Figure 6, note that clock 100 is the first active pixel, as the first 100 clocks produce dummy pixels (the output of the first 100 clocks should not be used for any purpose such as black level clamping).

Figure 7 shows the timing of the SO signal for the 400 dpi, 300 dpi, 200 dpi and 100 dpi modes, which corresponds with the 208th pixel for the 400 dpi mode, 150th pixel for the 300 dpi mode, the 92nd pixel for the 200 dpi mode and 34th pixel for 100 dpi mode. The sensor's SO signal can be used to determine when the end of the scan is reached. The last active pixel the sensor is the 232th pixel for the 400 dpi mode, 174th pixel for the 300 dpi mode, the 116th pixel for the 200 dpi mode and 58th pixel for the 100 dpi mode.

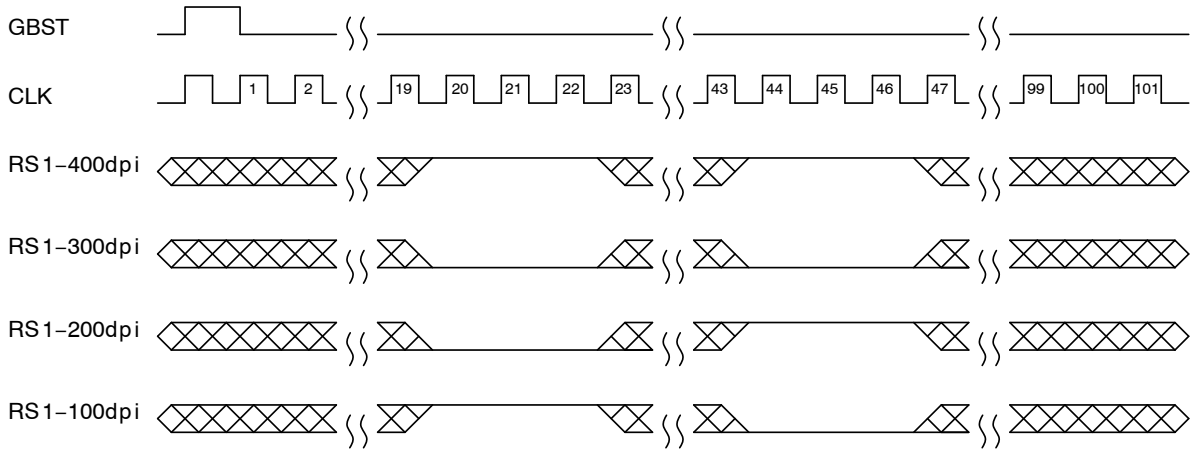


Figure 9. Resolution Select Input Timing

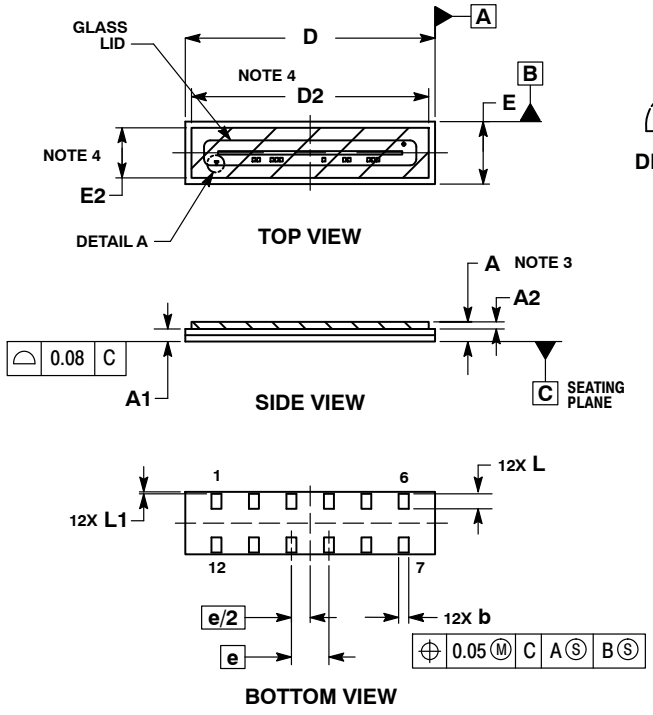
ORDERING INFORMATION

Device	Package	Temperature Range	Shipping†
NOP04811CLTAG	OLCC12 (Pb−Free)	−40°C to +85°C	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

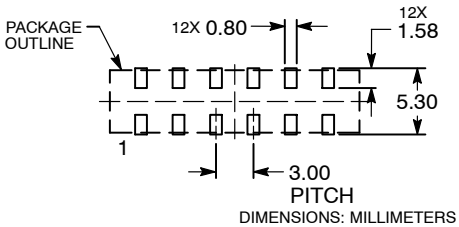
OLCC12 20x5, 3.0P
CASE 755AA
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT DOES NOT INCLUDE HEATSINKS OR OTHER ATTACHED FEATURES.
4. THE GLASS LID DEFINED BY DIMENSIONS D2 AND E2 MUST BE LOCATED WITHIN DIMENSIONS D AND E.
5. PIN ONE INDICATOR SHALL BE AS SHOWN IN THIS LOCATION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.37	1.77
A1	1.00 REF	
A2	0.50 REF	
b	0.75	0.85
D	19.90	20.10
D2	19.00 REF	
E	4.90	5.10
E2	4.00 REF	
e	3.00 BSC	
L	1.15	1.25
L1	0.10	0.20

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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